

FIG. 1 PRIOR ART

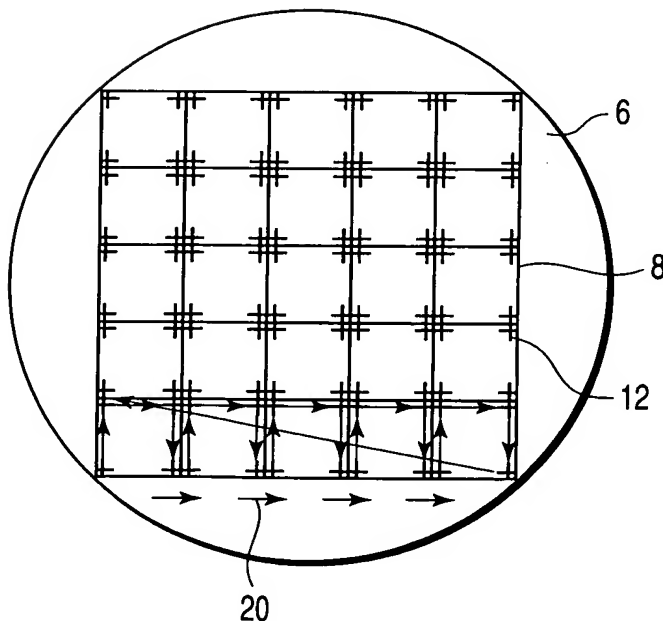


FIG. 2A

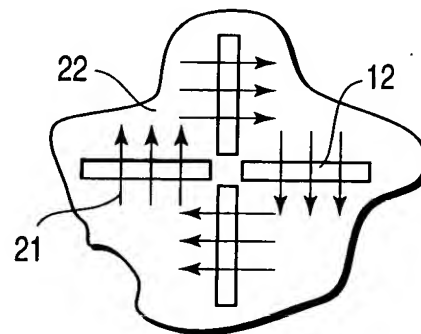


FIG. 2B

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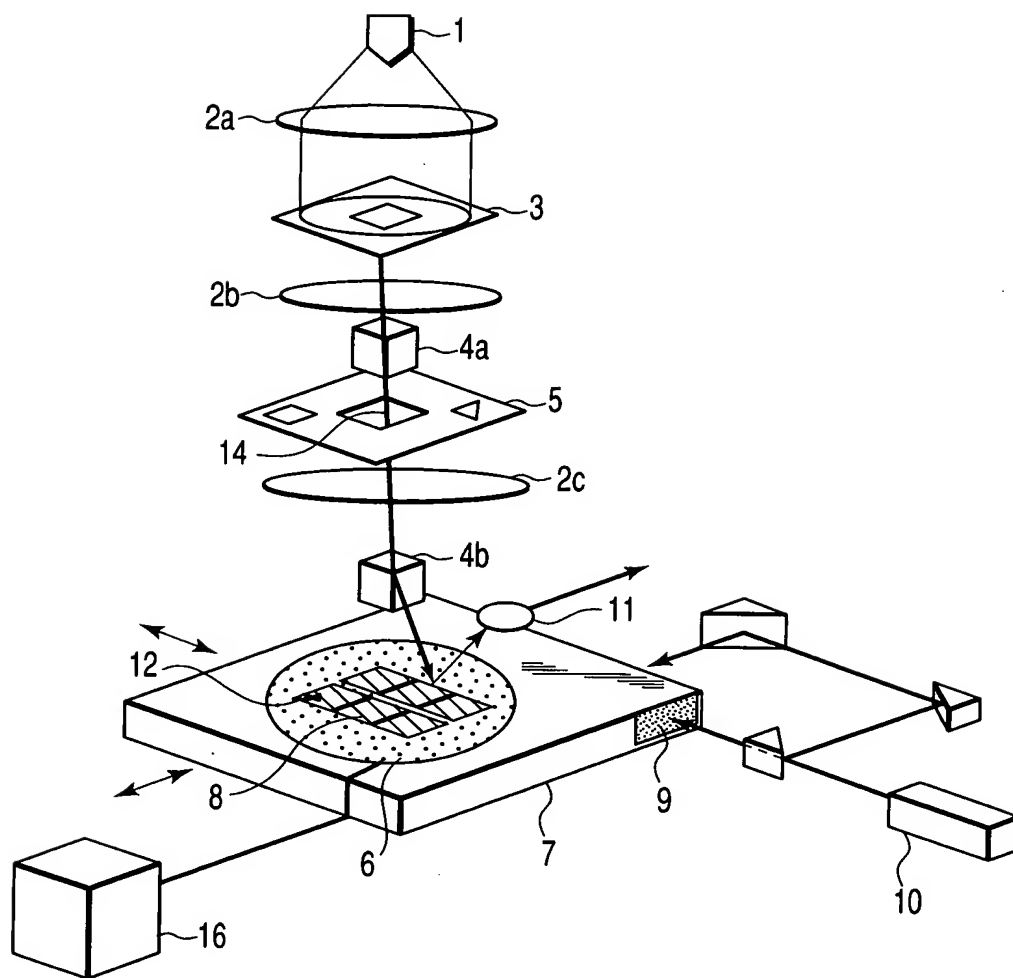


FIG. 3A

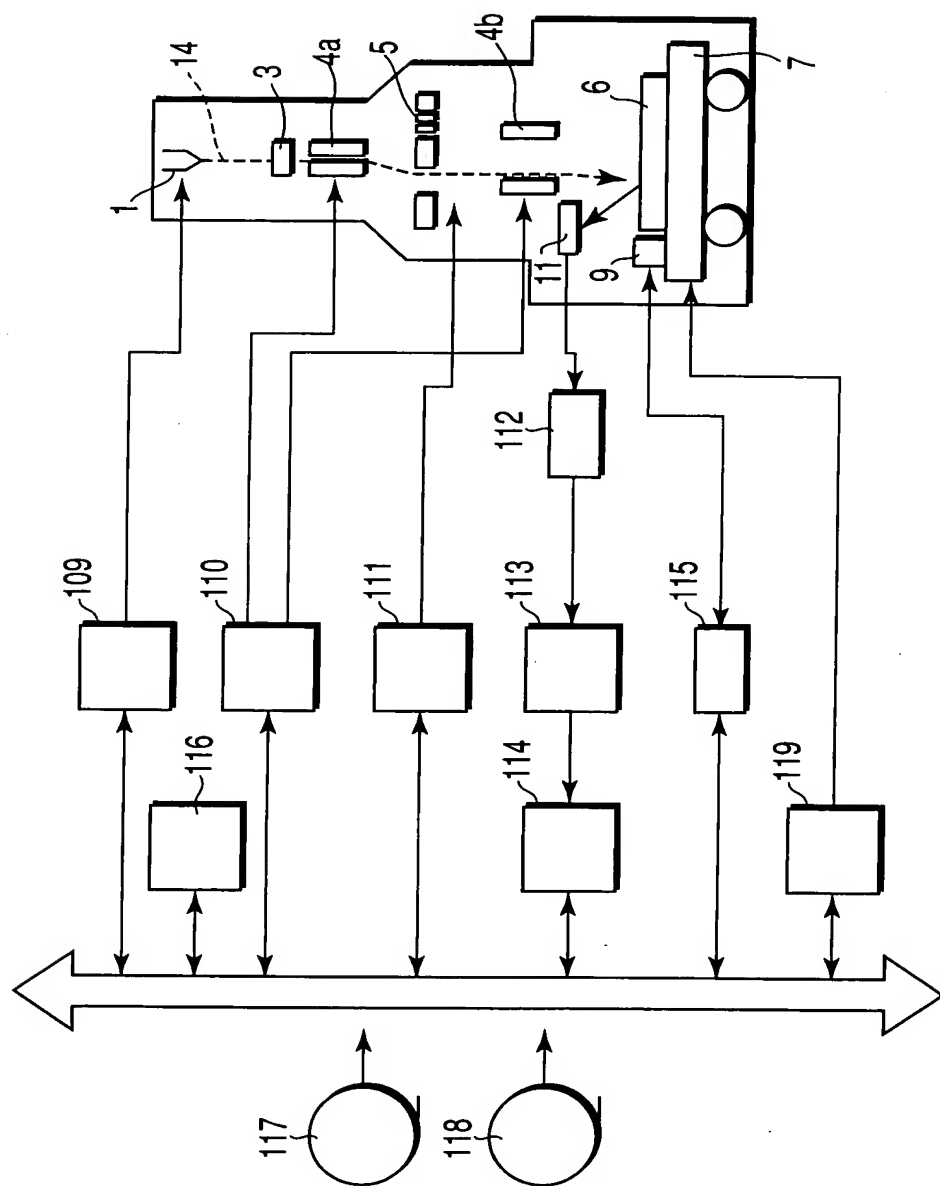
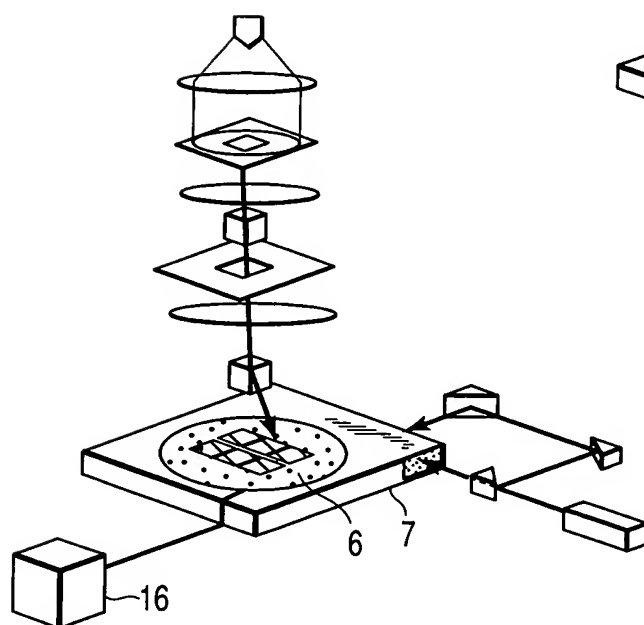
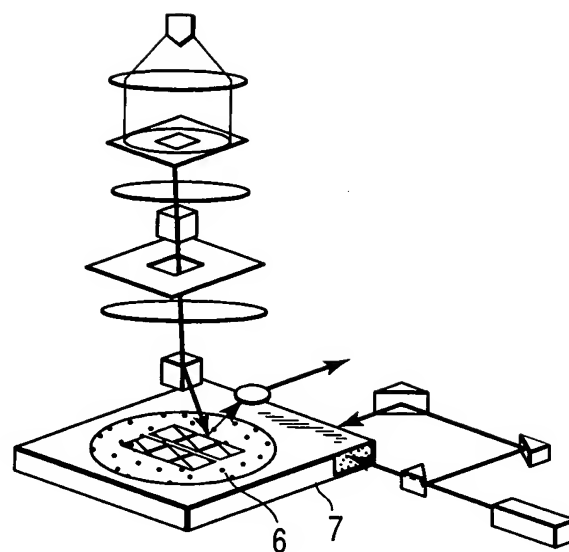
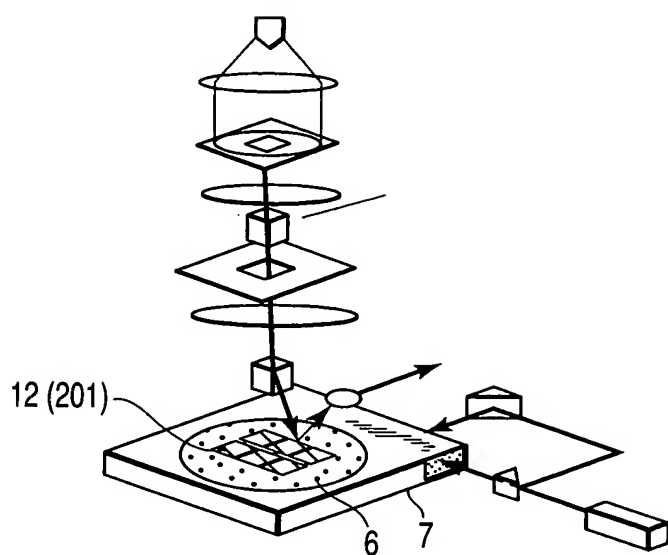


FIG. 3B



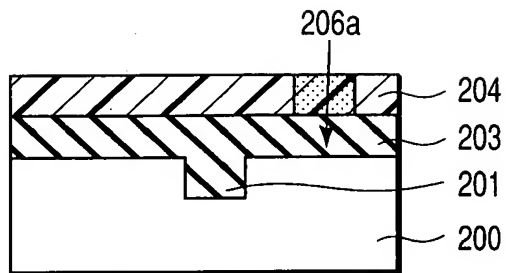


FIG. 5A

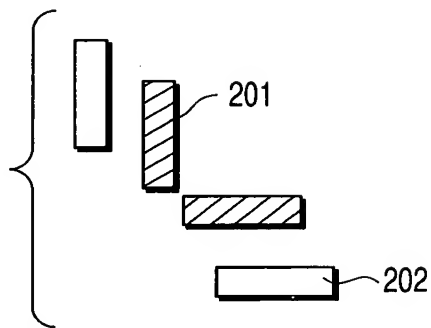


FIG. 5B

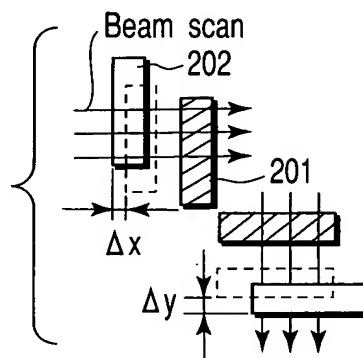


FIG. 5C

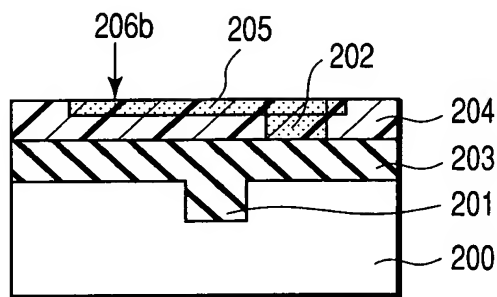


FIG. 5D

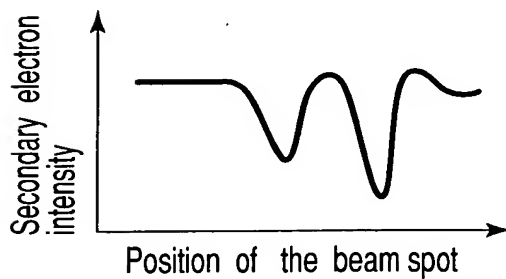


FIG. 5E

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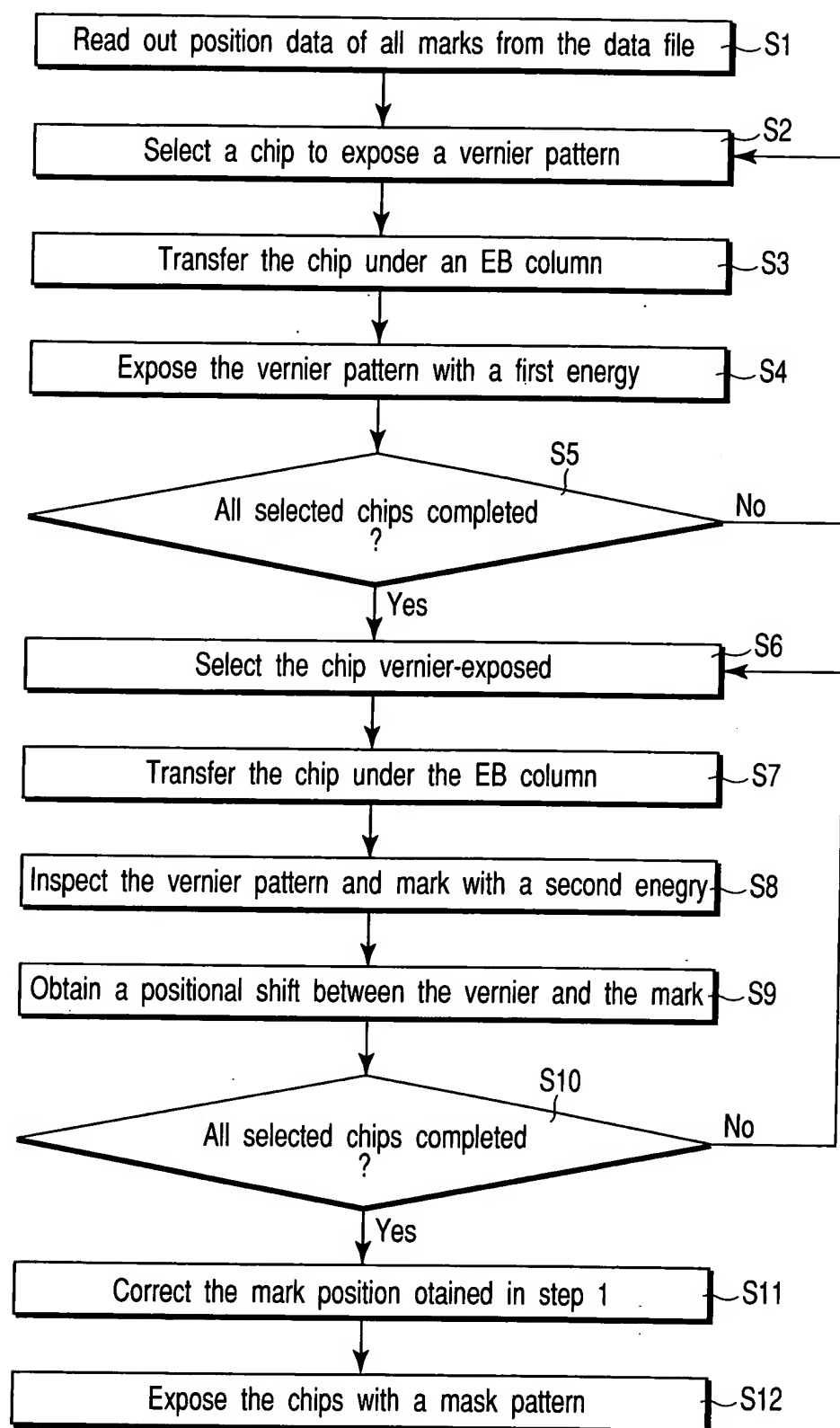
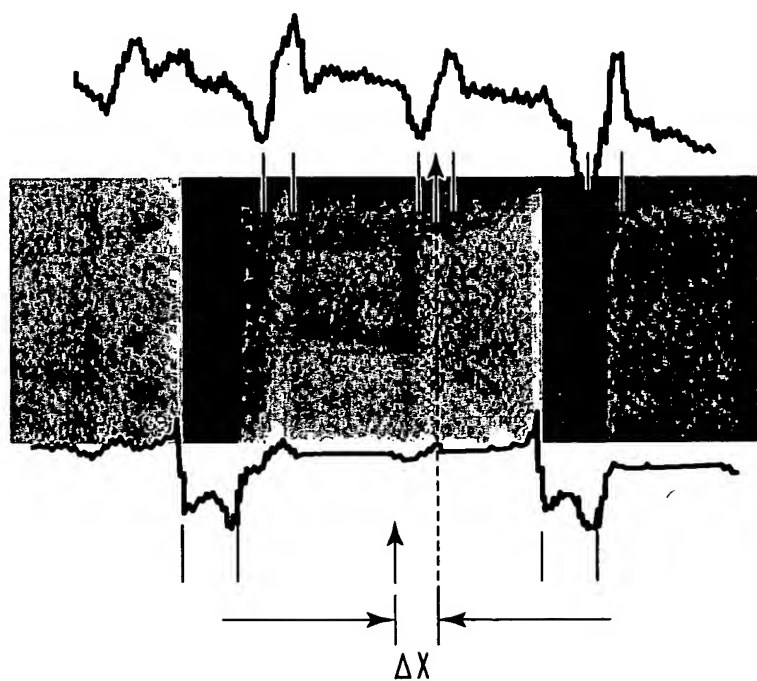
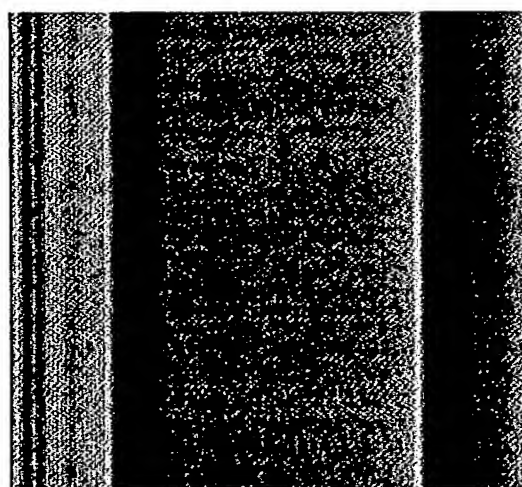


FIG. 6

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F I G. 7



Mark image

F I G. 9B

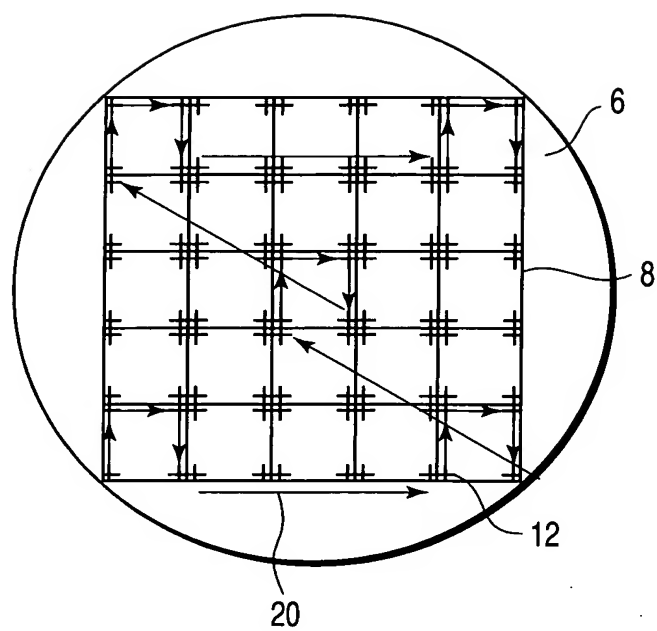


FIG. 8

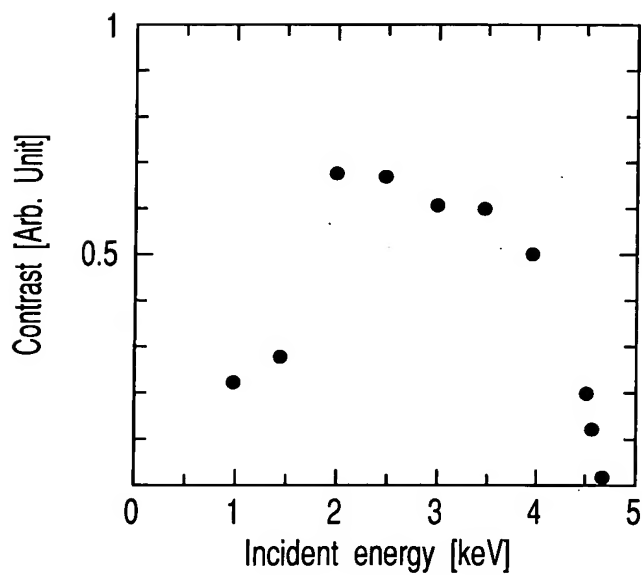


FIG. 9A


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graph TD
    S1[Select a chip for position detection] --> S2[Transfer the chip under an EB column]
    S2 --> S3[Detect a mark position of the chip]
    S3 --> S4{All selected chips completed?}
    S4 -- No --> S1
    S4 -- Yes --> S5[Calculate positional shift of all chips]
    S5 --> S6[Select a chip to expose a vernier pattern]
    S6 --> S7[Expose the vernier pattern with a first energy]
    S7 --> S8{All selected chips completed?}
    S8 -- No --> S6
    S8 -- Yes --> S9[Selected the chip vernier-exposed]
    S9 --> S10[Transfer the chip under the EB column]
    S10 --> S11[Inspect the vernier pattern and mark with a second energy]
    S11 --> S12[Obtain positional shift between the vernier and the mark]
    S12 --> S13{All selected chips completed?}
    S13 -- No --> S9
    S13 -- Yes --> S14[Correct the mark position obtained in step 5]
    S14 --> S15[Expose the chips with a mask pattern]
  
```

FIG. 10

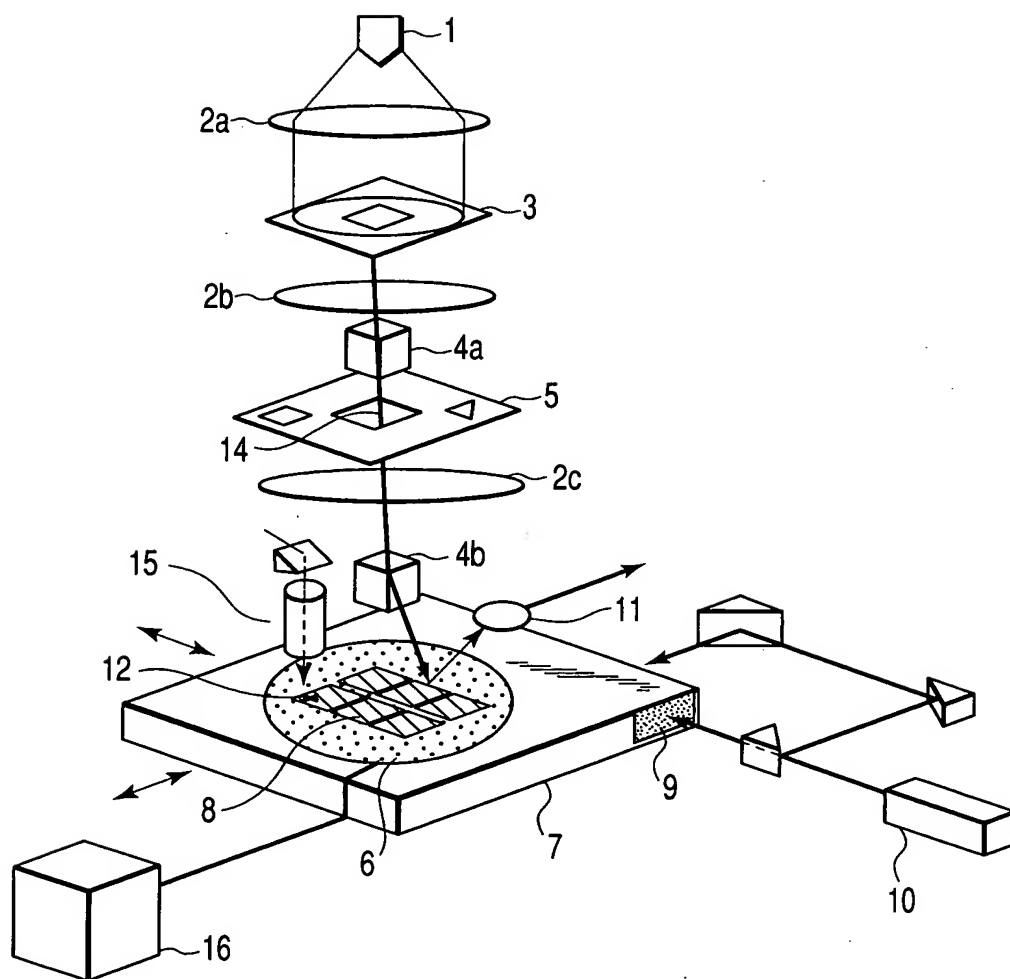


FIG. 11

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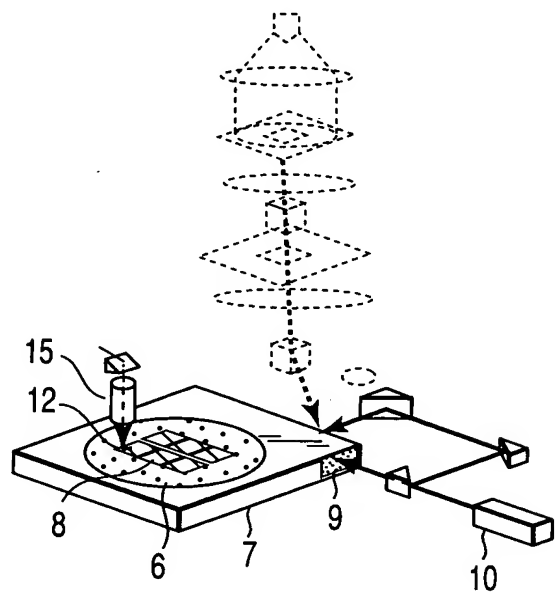


FIG. 12A

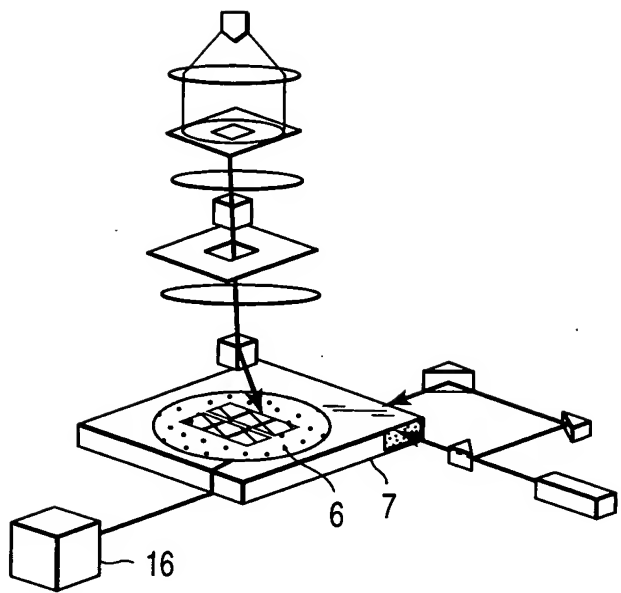


FIG. 12C

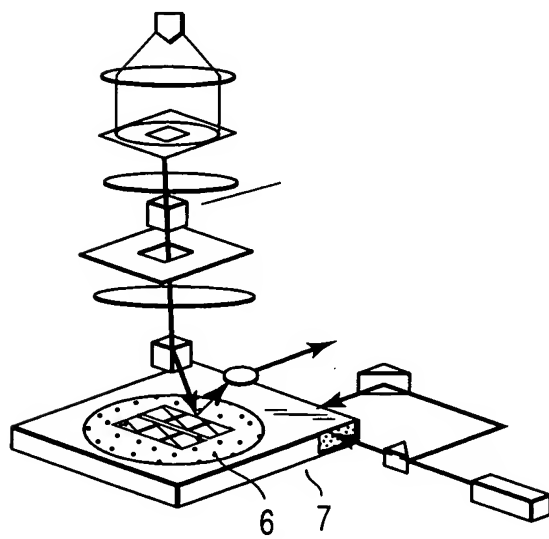


FIG. 12B

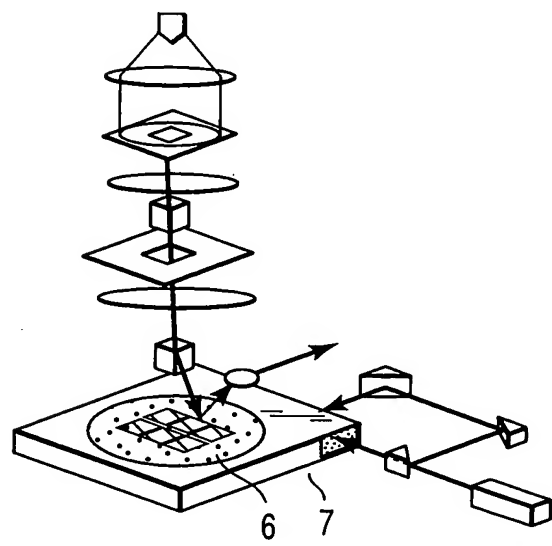


FIG. 12D

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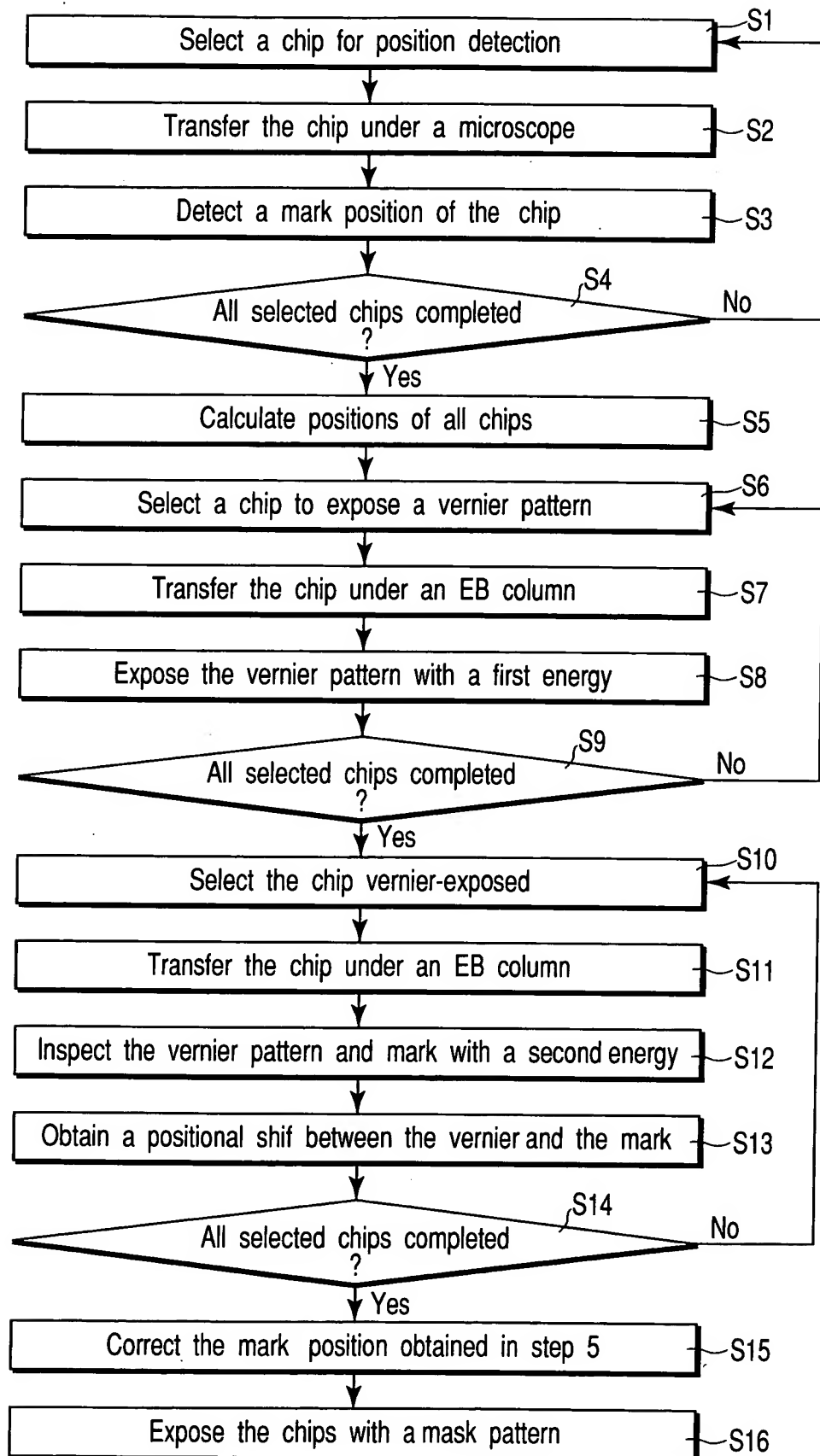


FIG. 13

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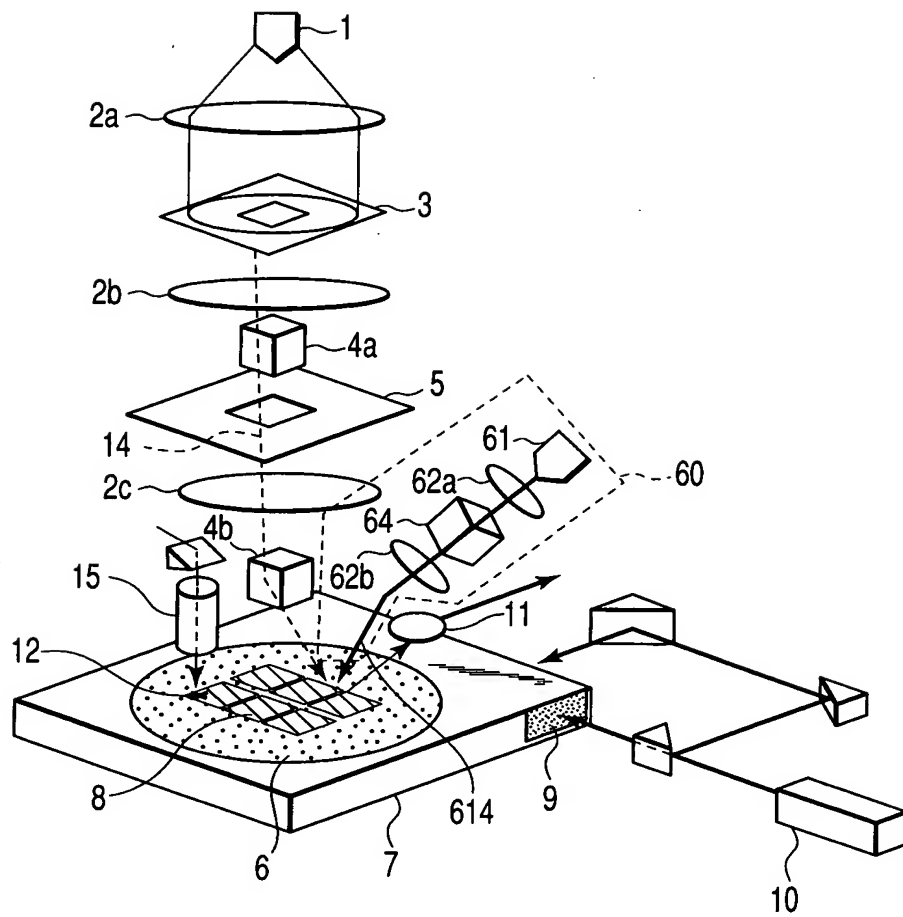


FIG. 14

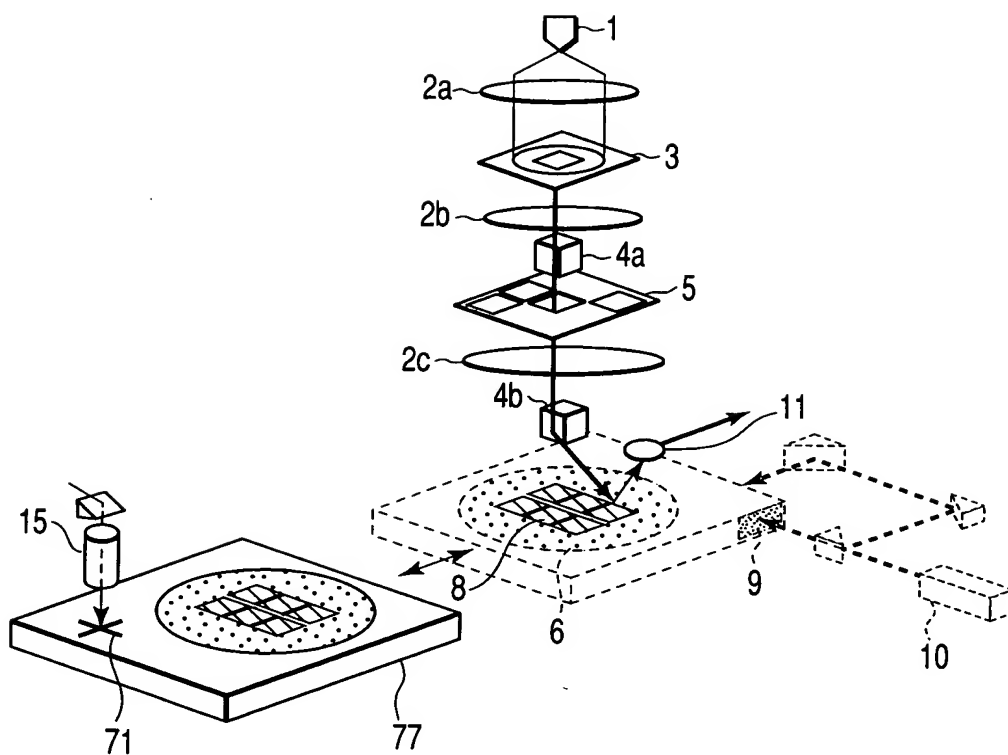


FIG. 15A

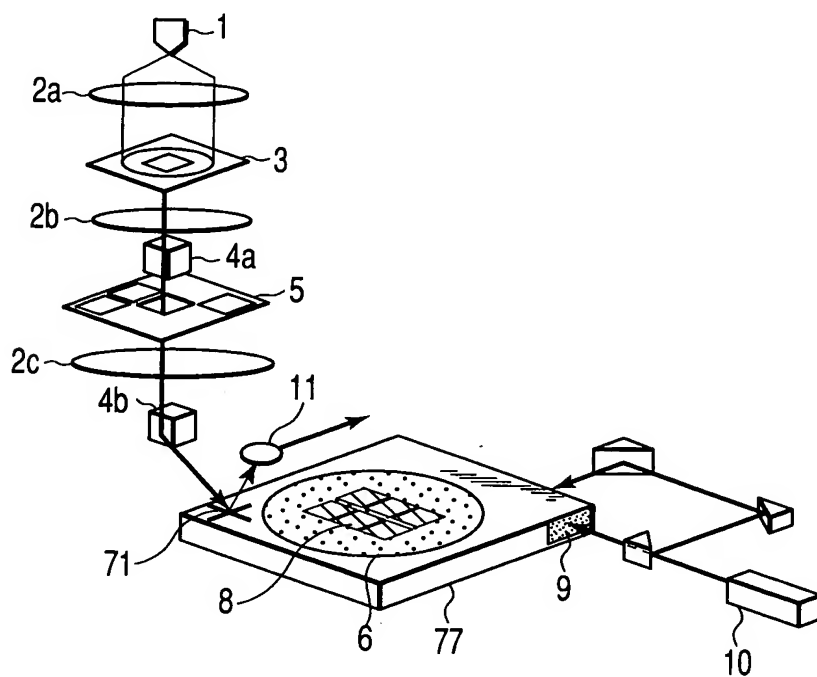


FIG. 15B

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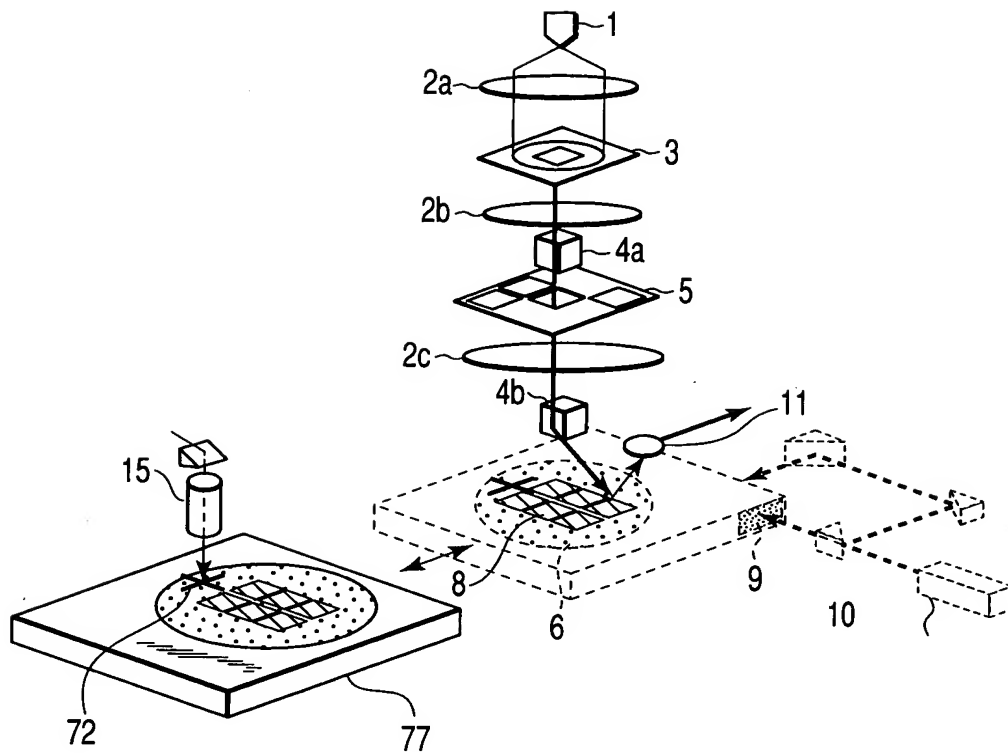


FIG. 16A

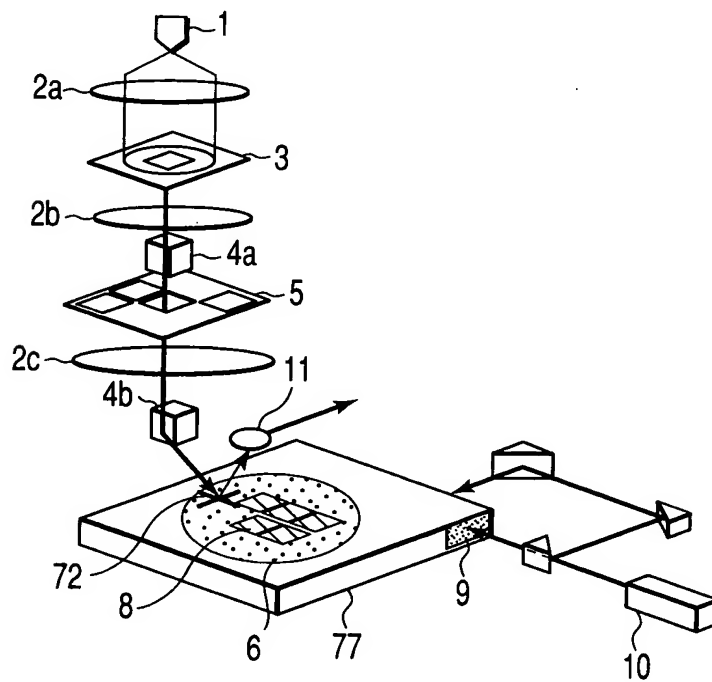


FIG. 16B

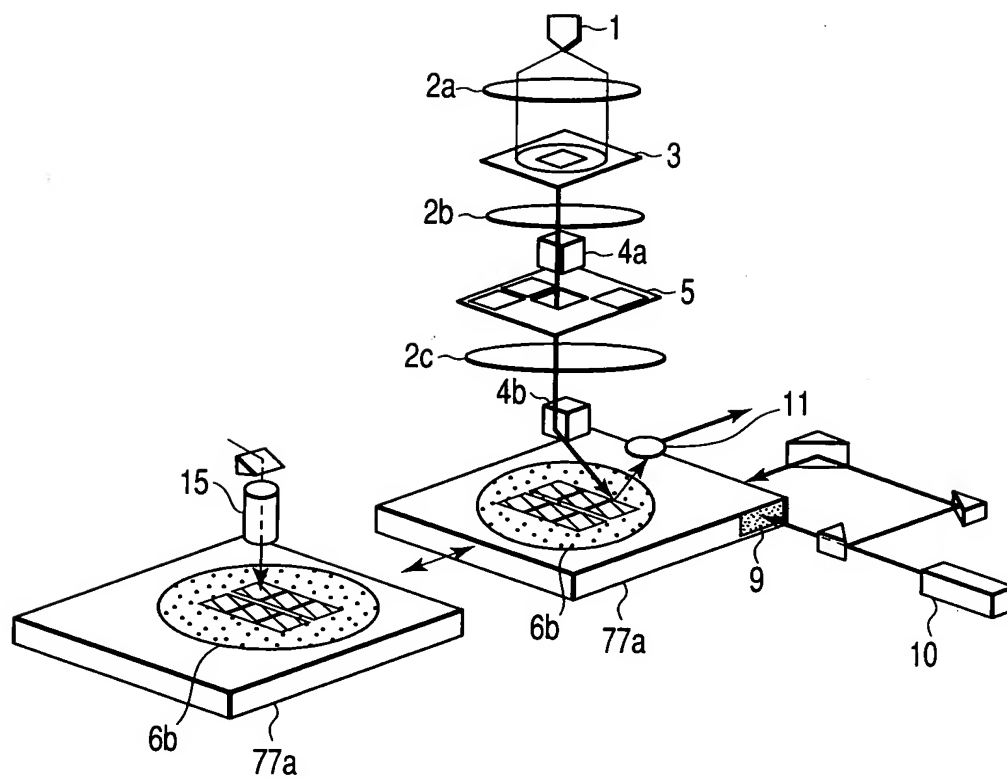


FIG. 17

FIG. 18A

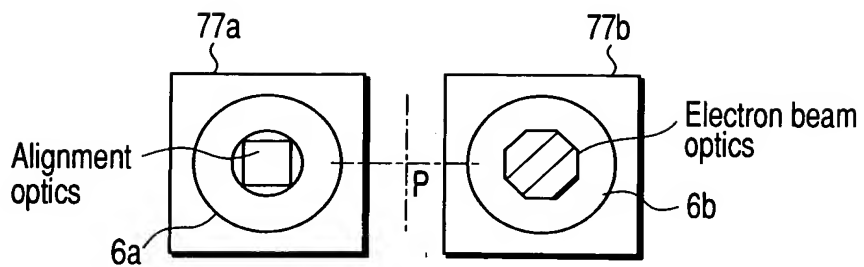


FIG. 18B

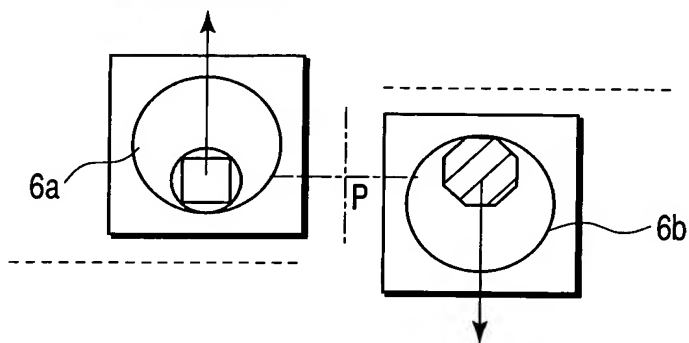


FIG. 18C

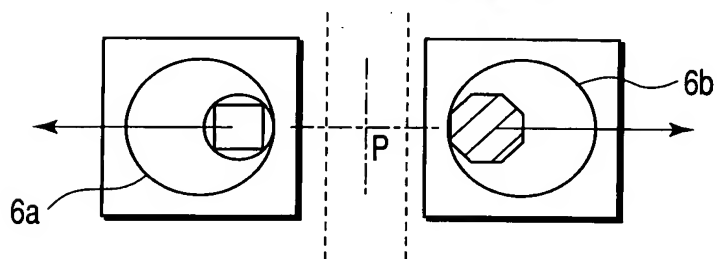


FIG. 19

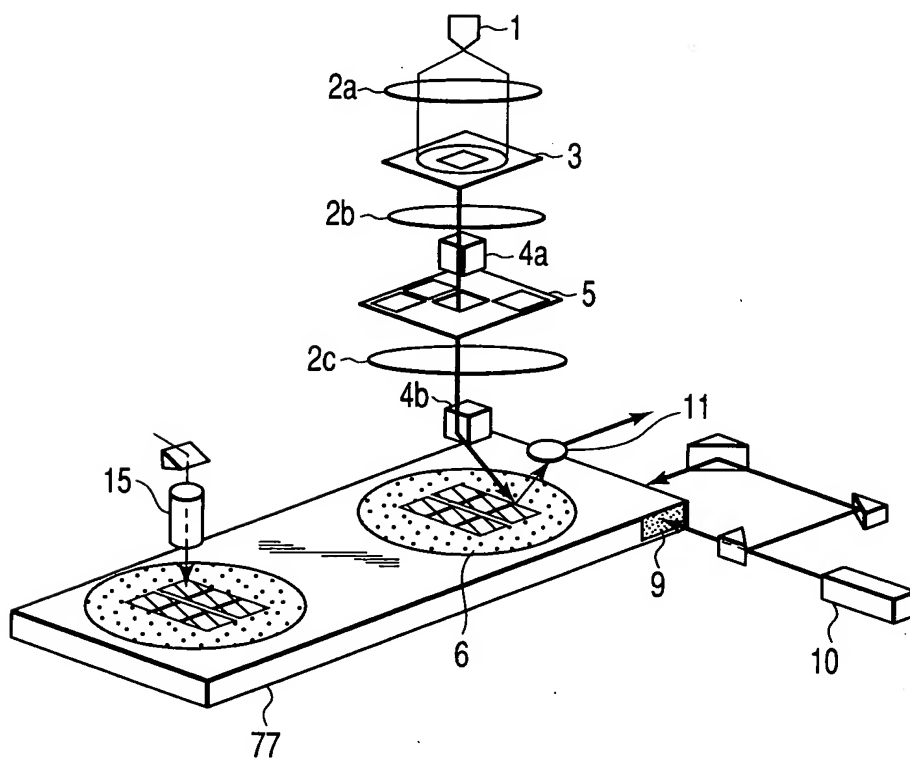


FIG. 20

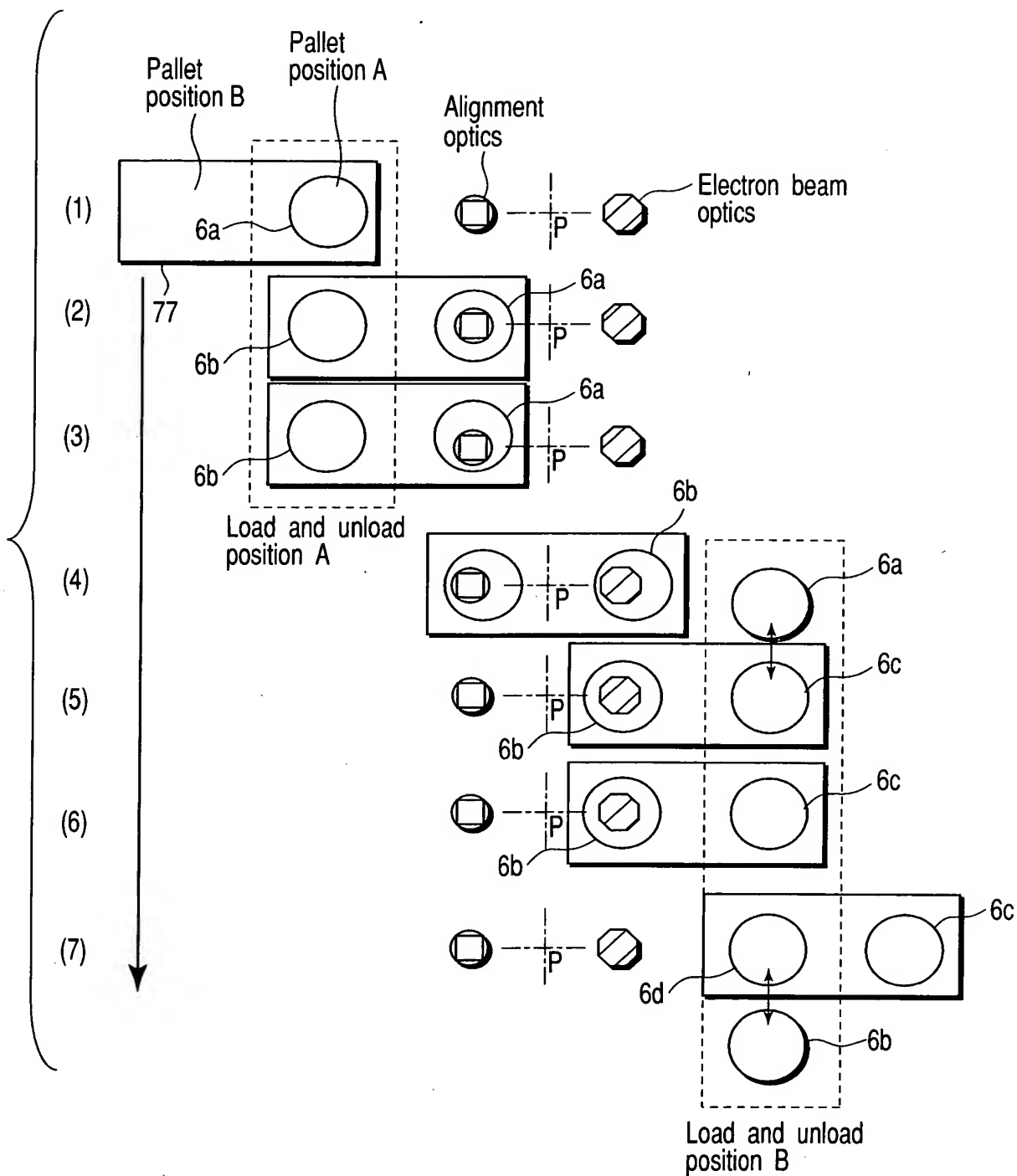


FIG. 20

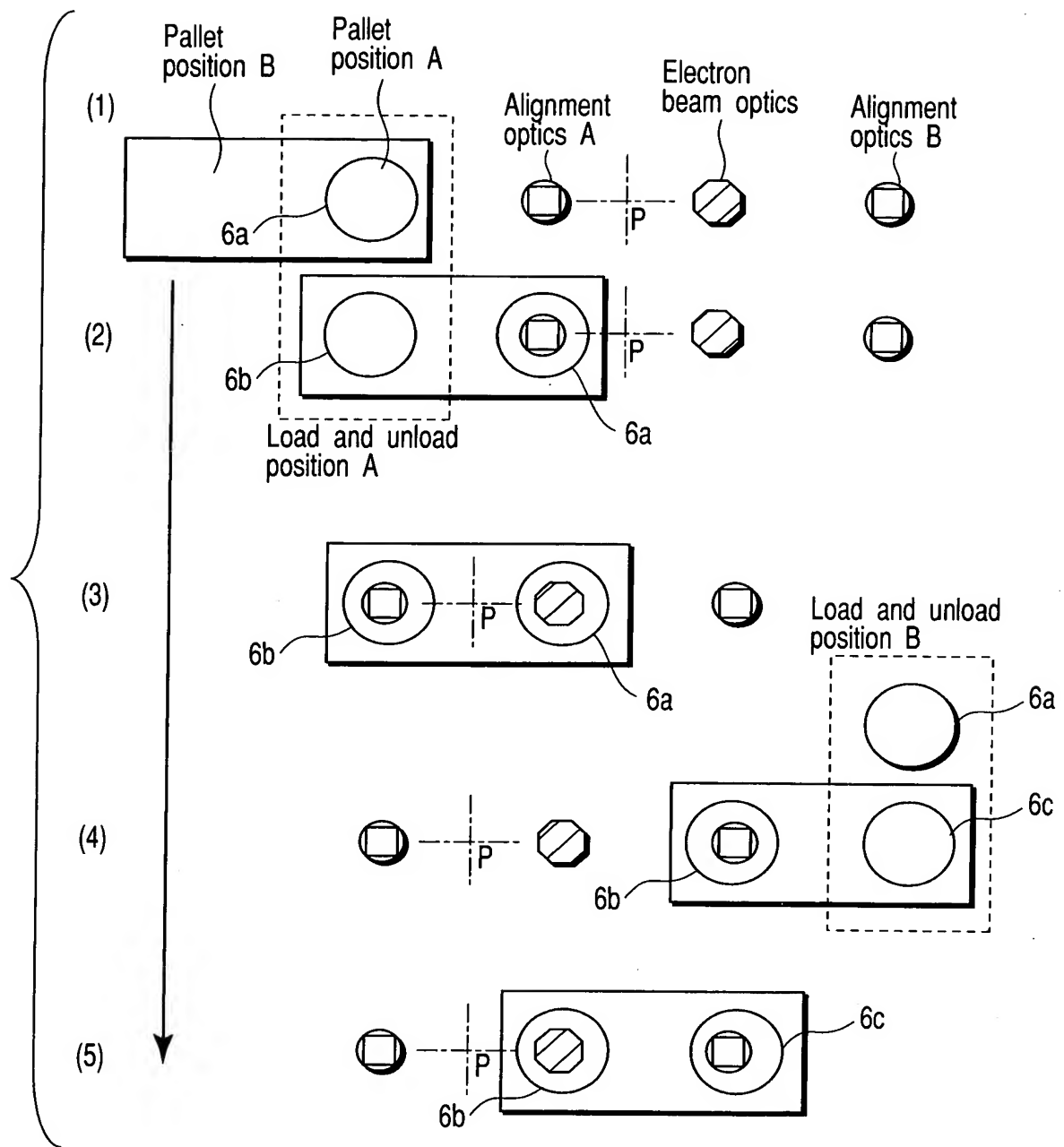
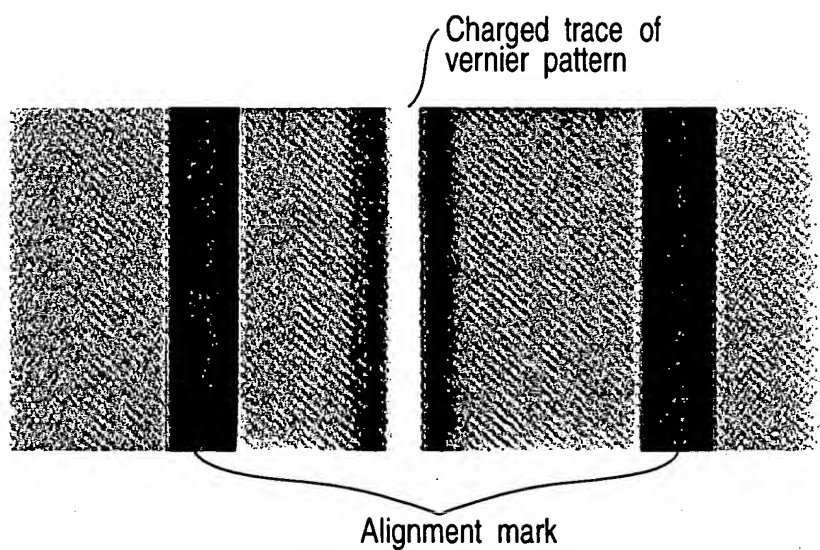


FIG. 21

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